1. Description

PSC2965 combines a highly integrated switch-mode charger, to minimize single-cell Lithium-ion (Li-ion) charging time from a USB power source, and a boost regulator to power a USB peripheral from the battery.

Its low impedance power path optimizes switch-mode operation efficiency, reduces battery charge time and extends battery life during discharging phase. The I2C serial interface with charging and system settings makes the device a truly flexible solution.

The device supports 4.5-13.5V input voltage sources, including standard USB host port and USB charging port with programmable over-voltage protection. The device also supports USB On-the-Go operation by providing on the VBUS with an accurate current limit.

The power path management regulates the system slightly above battery voltage but does not drop below 3.55V minimum system voltage (programmable). With this feature, the system keeps operating even when the battery is completely depleted or removed. When the input source current or voltage limit is reached, the power path management automatically reduces the charge current to zero and then starts discharges the battery until the system power requirement is met. This supplement mode operation keeps the input source from getting overloaded.

The device initiates and completes a charging cycle when host control is not available. It automatically charges the battery in three phases: pre-conditioning, constant current, and constant voltage. In the end, the charger automatically terminates when the charge current is below a preset limit in the constant voltage phase. Later on, when the battery voltage falls below the recharge threshold, the charger automatically starts another charging cycle.

The charge device provides various safety features for battery charging and system operation, including charging safety timer, and over-voltage/over-current protections.

The STAT output reports the charging status. The INT output can be used to notify the host when VBUS insertion and withdrawal or a fault occurs.

The PSC2965 is available in a 24-pin, 4mm x 4mm x 0.55mm QFN package.

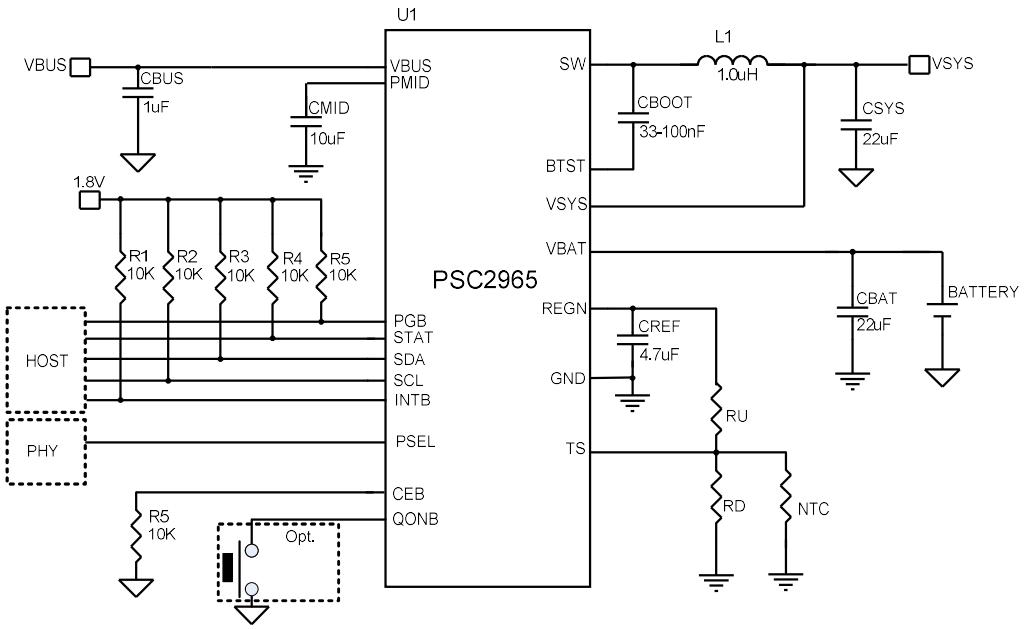


Figure 1.1 Typical Application

Key Components	Recommended specification
L1	Inductor, 1.0-2.2uH, +-20%, Isat>4A
C_{MID}	Capacitor, 10μF , +-10%, >16V
C_{REF}	Capacitor, 4.7μF, +-10%, >6V
C_{BUS}	Capacitor, 1.0μF, +-10%, >16V
C_{BOOT}	Capacitor, 100nF, +-10%, >10V

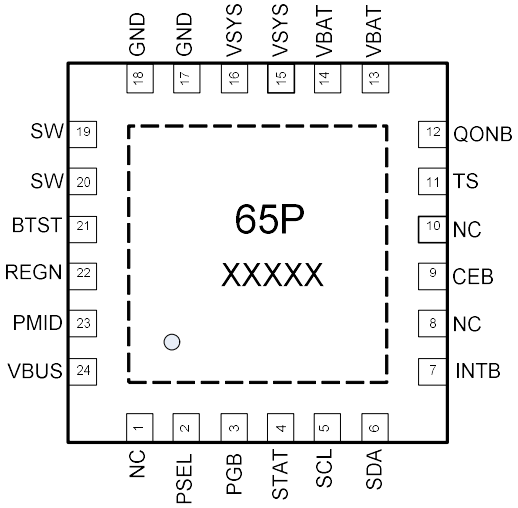
2. Features

- Fully Integrated, High-Efficiency Switching Mode 3A Charger.
  - Charge Voltage Accuracy: ±0.5% 25℃
  - ±7.5% Charge Current Regulation Accuracy
  - 20V Absolute Maximum Input Voltage
  - 13.5V Maximum Input Operating Voltage
  - Weak Input Sources Accommodated by Reducing Charging Current to Maintain Minimum VBUS Voltage
- Power Path Management
  - Instant system on with NO battery or deeply discharged battery
  - Battery can be completely turned off after Charging Done
  - Supports Ultra low leakage ship mode
- Programmable through I2C Interface:
  - Input Current limit
  - Fast-Charge/Termination Current
  - Charger Voltage
  - Termination Enable
- Small Footprint 1-2.2μH External Inductor
- Low Reverse Leakage to Prevent Battery Drain to VBUS
- High Battery Discharge Efficiency With 35mΩ Battery Discharge MOSFET
- High Integration Includes All MOSFETs, Current Sensing and Loop Compensation
- 30μA Low Battery Leakage Current to Support Ship Mode
- 45uA Low Battery Leakage Current in standby Mode
- 5V, 1A Boost Mode for USB OTG: 92% efficiency at 5V/1A
- QFN4x4-24L package

3. Applications

- Cellular Phones, Smart Phones, PDAs
- Tablet, Portable Media Players

4. Pin Configuration and Functions



65P: Product ID
XXXXX: Production Tracing Code

Figure 4.1 QFN4X4-24L TOP view

Pin functions

Name	Pin #	Type	Description
VBUS	24	P	Charger Input Voltage. Place a 1-μF ceramic capacitor from VBUS to GND and place it as close as possible to IC.
-	1,8,10	-	NC.
PSEL	2	DI	Power source selection input, active by PSEL_EN=1 . Set 500 mA input current limit by pulling this pin high and set input current limit by Reg00[4:0] by pulling this pin low.
PGB	3	DO	Open drain active low power good indicator. Connect to the pull up rail through 10-kΩ resistor. LOW indicates a good input source if the input voltage is between UVLO and OVP threshold, above SLEEP mode threshold..
STAT	4	DO	Open drain charge status output to indicate charger status. HIGH indicates charge disabled.
SCL	5	DI	I^2C Interface clock. Connect SCL to the logic rail through a 10-kΩ resistor.
SDA	6	DIO	I^2C Interface data. Connect SDA to the logic rail through a 10-kΩ resistor.
INTB	7	DO	Open-drain interrupt Output. The INT pin sends an pulse to host to report charger device status and fault.
CEB	9	DI	Charge Enable pin. Battery charging is enabled when this pin is driven low. Battery charging and Vsys regulator are disable when CEB is high.

Name	Pin #	Type	Description
TS	11	AI	Temperature qualification voltage input. Connect a negative temperature coefficient thermistor between TS and GND. 103AT-2 thermistor is preferred.
QONB	12	DI	BATFET enable/reset control input. The pin contains internal pull-up so it could be floating if it is not used. Pull down QONB for about 430ms will turn on BATFET and exit ship mode. When VBUS is not valid, a logic low of typically 10s duration cuts VSYS from VBAT for 430ms and then re-enables BATFET to provide full system power reset.
VBAT	13,14	P	Battery connection point to the positive pin of the battery pack. The internal Q4 is connected between VBAT and VSYS. Connect a 22 μF Capacitor closely to the VBAT pin.
VSYS	15,16	P	System power supply. Connect a 22 μF capacitor closely to the VBAT pin.
GND	17,18	-	Power ground connection for high-current power converter node. On PCB layout, connect directly to ground connection of input and output capacitors of the charger. A single point connection is recommended between power PGND and the analog GND near the IC PGND pin.
SW	19,20	P	Switching node connecting to output inductor. Internally SW is connected to the source of the High-side NMOS and the drain of the low-side NMOS.
BTST	21	P	PWM high side driver positive supply. Internally, the BTST is connected to the anode of the boost-strap diode.
REGN	22	P	PWM low side driver positive supply output. Internally, REGN is connected to the cathode of the boost- strap diode.
PMID	23	DO	Power input to the charge regulator. Connect a 10uF ceramic capacitor from PMID to analog GND.
Thermal PAD	Thermal PAD	P	Exposed pad for heat dissipation. Always solder thermal pad to the board, and have via on the thermal pad plane star-connecting to GND.

5. Specifications

5.1 Maximum Ratings and Thermal Characteristics

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Parameter (TA=25℃ unless otherwise noted**)**		**Symbol**	**Min.**	**Max.**	**Units**
VBUS Voltage	Continuous	V_{BUS}	-0.3	20	V
STAT, INTB Voltage		V_{STAT}	-0.3	7	V
PMID		V_I	-0.3	20	V
SW Voltage			-0.3	18	
VSYS, VBAT, REGN, CEB Voltage			-0.3	7	
Voltage on Other Pins		V_O	-0.3	6.5(1)	V
Electrostatic Discharge Protection Level	Human Body Model	ESD	2000		V
	Charged Device Model		500		
Junction Temperature		T_J	-40	+150	℃
Storage Temperature		T_{STG}	-65	+150	℃
Lead Soldering Temperature, 10 Seconds		T_L		+260	℃

(1) Lesser of 6.5V or V_I + 0.3V.

5.2 Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Prisemi does not recommend exceeding them or designing to absolute maximum ratings.

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{BUS}	4.5	13.5	V
Maximum Battery Voltage when Boost enabled	$V_{BAT(MAX)}$		4.5	V
Input Current	Iin		3.2	A
Output Current	Isys		3	A
Fast Charging Current			3	A
Discharge Current thru internal MOSFET			6	A
Ambient Temperature	T_A	-40	+85	℃
Junction Temperature (see Thermal Protection section)	T_J	-40	+140	℃

5.3 Thermal Properties

Junction-to-ambient thermal resistance is a function of application and board layout. This data is measured with four-layer 2s2p boards in accordance to JEDEC standard JESD51. Special attention must be paid not to exceed junction temperature $T_{J(max)}$ at a given ambient temperature T_A.

Parameter	Symbol	Typical	Units
Junction-to-Ambient Thermal Resistance	θ_{JA}	35	℃/W
Junction-to-PCB Thermal Resistance	θ_{JB}	10	℃/W

5.4 Electrical Characteristics

Unless otherwise specified: according to the circuit of Fig.1.1; recommended operating temperature range for T_J and T_A; V_{BUS}=5.0V, Charge Mode; and typical values are for T_J=25℃.(Unless otherwise noted.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
QUIESCENT CURRENTS						
VBUS Current	I_{VBUS}	V_{BUS}>$V_{BUS(MIN)}$, PWM Switching V_{BUS}=12V		1.2		mA
		V_{BUS}>$V_{BUS(MIN)}$; PWM Enabled, Not Switching ;V_{BUS}=12V		1.2		mA
HZ Input Current	I_{HZ}	HZ Mode, No Battery		660	800	μA
Battery Leakage	I_{BAT}	VBAT = 4.2 V, No VBUS, Not in boost mode, BATFET Disabled. Ta < 85°C		30	40	μA
Battery Leakage	I_{BAT}	VBAT = 4.2 V, No VBUS, Not in boost mode, BATFET Enabled. Ta < 85°C		45	58	μA
BATTERY CHARGER						
Charge Voltage Range	V_{OREG}		3.984		4.464	V
Charge Voltage Accuracy		Ta=25℃	-0.5		+0.5	%
		Ta=-40~85℃	-1		1	%
Output Charge Current Range	I_{OCHRG}	V_{LOWV} < V_{BAT} < V_{OREG}			3000	mA
Charge Current Accuracy		T_a<85℃,VBAT=3.8V REG02[5:0]=100000,ICHG=1.92A	-7.5		+7.5	%
Pre-charge Current	I_{PRECHG}	REG03[7:4]=0000		60		mA
		REG03[7:4]=0010		180		
		REG03[7:4]=0100		300		
		REG03[7:4]=1000		540		
Linear Charging Current	I_{SHORT}		15	20	25	mA
Battery Short Voltage	V_{SHORT}		1.9	2.05	2.2	V
Termination Current Range	$I_{(TERM)}$	V_{BAT} > V_{OREG} – V_{RCH}	100		800	mA
Wake-up voltage Range	V_{wakeup}	Pre-Charge Current if VBAT is lower than V_{wakeup}	2.95	3.1	3.25	V
VBUS Operating Voltage	V_{IN_VALID}	Valid VBUS voltage for charging	4.5		13.5	V
VBUS Validation Time	t_{VBUS_VALID}			40		ms

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Voltage Regulation Range	V_{INDPM}		4.0		5.5	V
Input Voltage Regulation Accuracy	V_{INDPM_ACC}		-3		+3	%
Recharge Threshold	V_{RCH}	Reg04[0]=0,Below $V_{(OREG)}$		100		mV
	t_{RCH}			10		ms
Sleep-Mode Entry Threshold, V_{BUS} – V_{BAT}	V_{SLP}	V_{BUS} Falling		100		mV
VBUS Over-Voltage Shutdown	$VBUS_{OVP}$	V_{BUS} Rising (I2C programmable)	5.5		13.8	V
Hysteresis		V_{BUS} Falling, VOVP=6.8V		100		mV
Accuracy		V_{BUS} Falling, VOVP=6.8V	-3		+3	%
Maximum Duty Cycle (charge)	D_{MAX}				98.5	%
POWER-PATH						
System regulation voltage range	V_{SYS_MIN}		3.2		3.7	V
System Regulation Voltage	V_{SYS_MAX}			4.5		V
SYS-BAT MOSFET on-resistance	$R_{ON(Q4)}$			35		mΩ
Q3 On Resistance (VBUS to PMID)	$R_{DS(ON)}$	$I_{IN(LIMIT)}$=500mA		45		mΩ
Q1 On Resistance (PMID to SW)				60		
Q2 On Resistance (SW to GND)				60		
BOOST MODE OPERATION						
Boost Output Voltage at VBUS	V_{BOOST}	3.3V<V_{BAT}<4.5V;	4.8	5.15	5.3	V
Boost Mode Quiescent Current	$I_{BAT(BST)}$	PFM Mode, V_{BAT}=4.2V, I_{OUT}=0		1.7		mA
Valley Current Limit (Q1)	$I_{LIM(BST)}$	Reg02[7]=0		0.8		A
		Reg02[7]=1		1.5		A
Current Limit (Q4)	$I_{LIM(BAT)}$			3.0		A
Min Battery Voltage for Boost	$UVLO_{BST}$			3.2		V
LOGIC I/O PIN CHARACTERISTICS						
High-Level Input Voltage	V_{IH}		1.2			V
Low-Level Input Voltage	V_{IL}				0.4	V
STAT Output Low	$V_{STAT(OL)}$	I_{STAT}=10mA			0.4	V
STAT High Leakage Current	$I_{STAT(OH)}$	V_{STAT}=5V			1	μA
THERMAL SHUTDOWN						
Thermal Shutdown Threshold(1)	$T_{SHUTDWN}$	T_J Rising		145		℃
Hysteresis(4)		T_J Falling		10		℃

(1) Guaranteed by design; not tested in production.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
JEITA Thermistor Comparator (BUCK MODE)						
Cold (0°C) threshold	T1	As Percentage to REGN		73.30		%
Falling				71.50		
Cool (10°C) threshold,	T2			68.00		
Falling				66.80		
Warm (45°C) threshold,	T3			44.70		
Falling				45.70		
Hot (60°C) threshold,	T5			34.20		
Falling				35.30		
Timing for QONB (external Key)						
QONB time to full system reset; BATFET switch on-off-on	Tqon_rst2			10		s
BATFET's off time during full system reset	Tqon_off			40		ms
QONB low time to exit ship mode	Tship_exit			160		ms

5.5 I2C Timing Specifications

Guaranteed by design.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
SCL Clock Frequency	f_{SCL}	Standard Mode			100	kHz
		Fast Mode			400	
Bus-Free Time between STOP and START Conditions	t_{BUF}	Standard Mode		4.7		μs
		Fast Mode		1.3		
START or Repeated START Hold Time	$t_{HD;STA}$	Standard Mode		4		μs
		Fast Mode		600		ns
SCL LOW Period	t_{LOW}	Standard Mode		4.7		μs
		Fast Mode		1.3		
SCL HIGH Period	t_{HIGH}	Standard Mode		4		μs
		Fast Mode		600		ns
Repeated START Setup Time	$t_{SU;STA}$	Standard Mode		4.7		μs
		Fast Mode		600		ns
Data Setup Time	$t_{SU;DAT}$	Standard Mode		250		ns
		Fast Mode		100		
Data Hold Time	$t_{HD;DAT}$	Standard Mode	0		3.45	μs
		Fast Mode	0		900	ns
SCL Rise Time	t_{RCL}	Standard Mode		$20+0.1C_B$	1000	ns
		Fast Mode		$20+0.1C_B$	300	
SCL Fall Time	t_{FCL}	Standard Mode		$20+0.1C_B$	300	ns
		Fast Mode		$20+0.1C_B$	300	
SDA Rise Time Rise Time of SCL after a Repeated START Condition and after ACK Bit	t_{RDA} t_{RCL1}	Standard Mode		$20+0.1C_B$	1000	ns
		Fast Mode		$20+0.1C_B$	300	

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
SDA Fall Time	t_{FDA}	Standard Mode	$20+0.1C_B$		300	ns
		Fast Mode	$20+0.1C_B$		300	
Stop Condition Setup Time	$t_{SU;STO}$	Standard Mode		4		μs
		Fast Mode		600		ns
Capacitive Load for SDA, SCL	C_B				400	pF

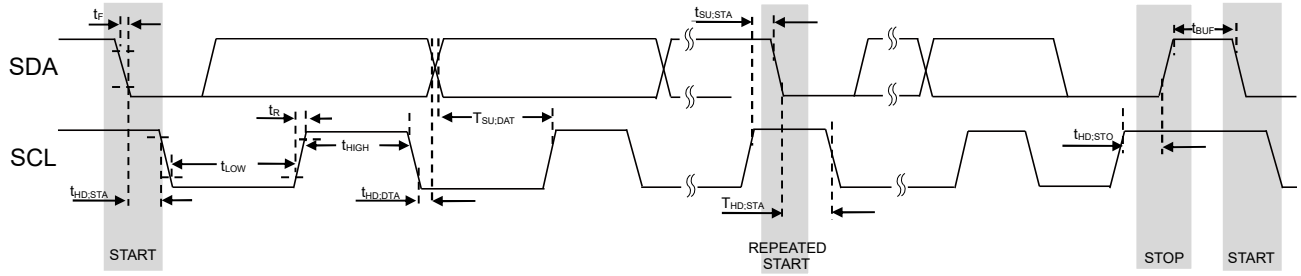


Figure 5.1 I²C Interface Timing for Fast and Slow Modes

5.6 Typical Performance Plots

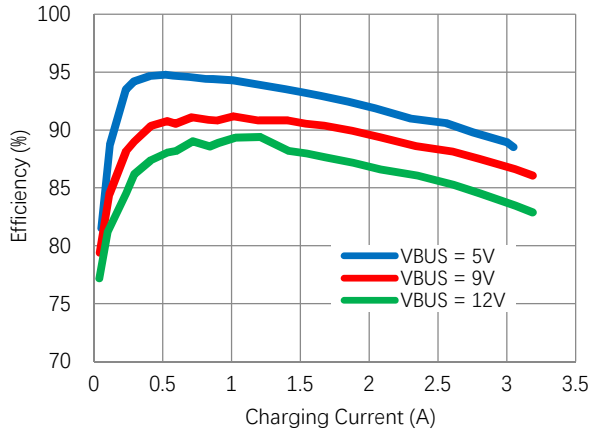


Fig1. Charge Efficiency vs. Charge Current

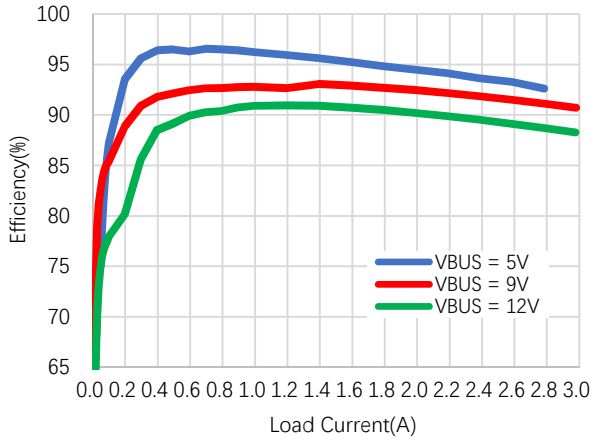


Fig2. System Efficiency vs. System Load Current

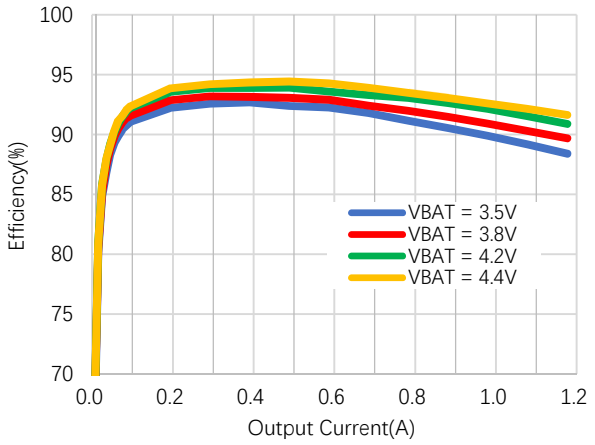


Fig3. Boost Mode Efficiency vs. VBUS Load Current

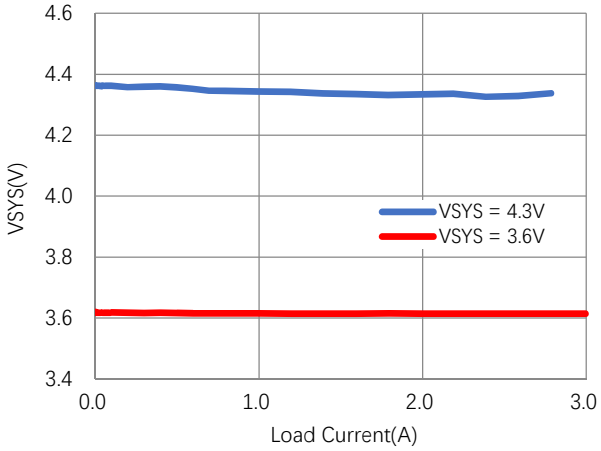


Fig4. VSYS Voltage Regulation vs. System Load Current

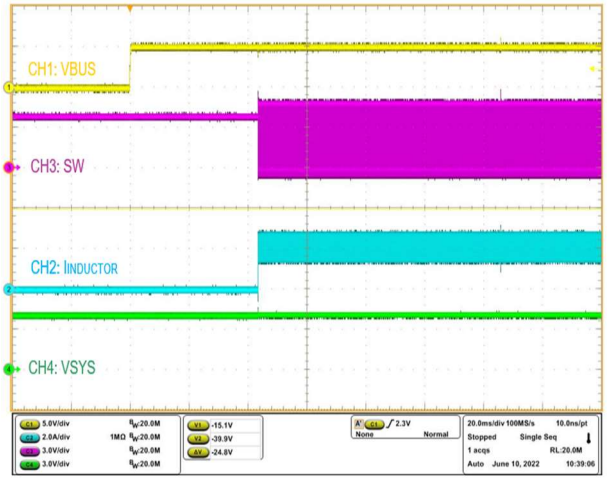


Fig5. Power on
(VBAT=3.8V,Icharge=2A)

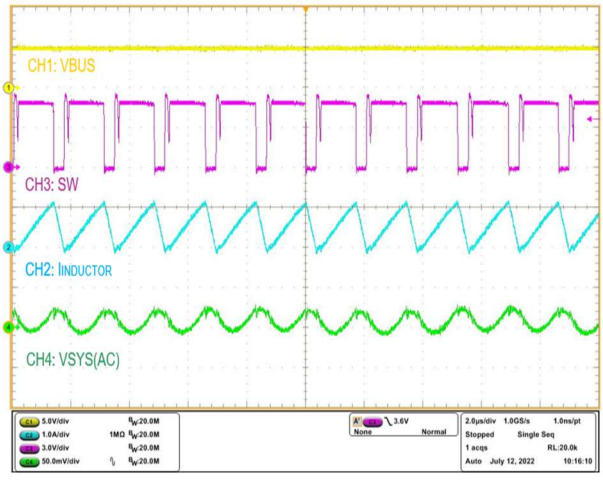


Fig6. Switching in Buck Mode
(Vbus=5V,Icharge=500mA)

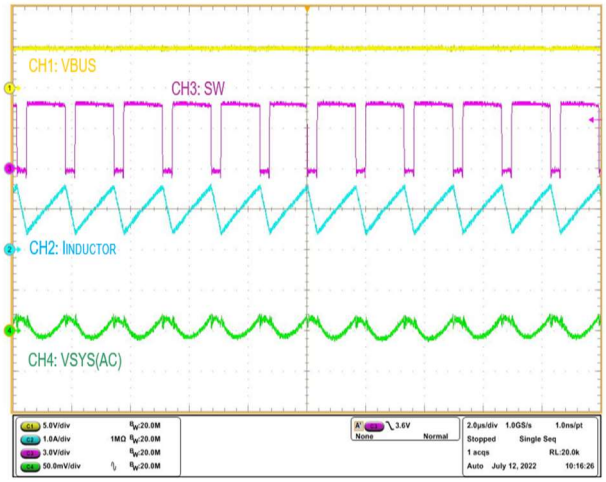


Fig7. Switching in Buck Mode
(Vbus=5V,Icharge=1A)

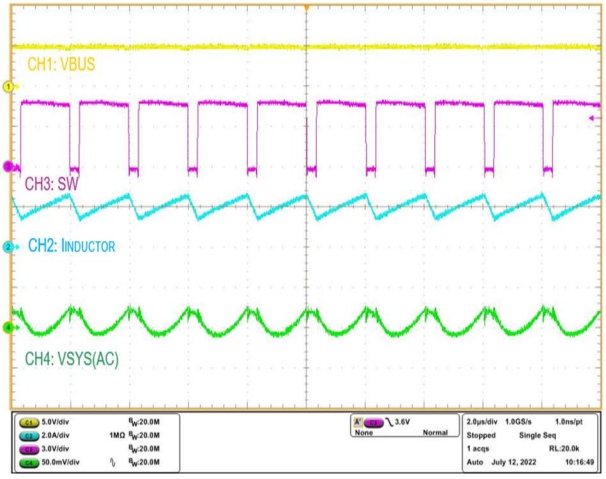


Fig8. Switching in Buck Mode
(Vbus=5V,Icharge=2A)

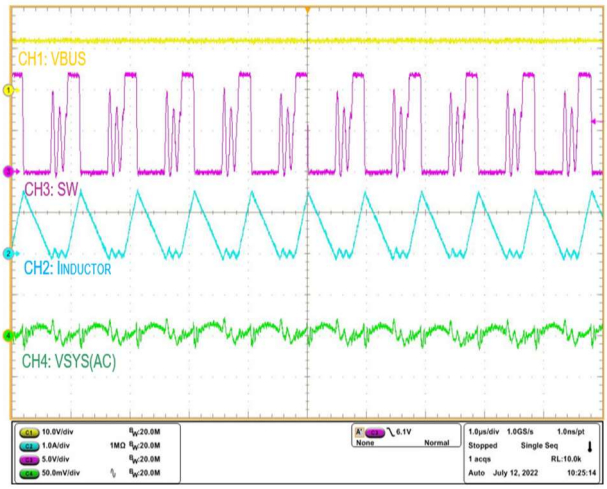


Fig9. Switching in Buck Mode
(Vbus=12V,Icharge=500mA)

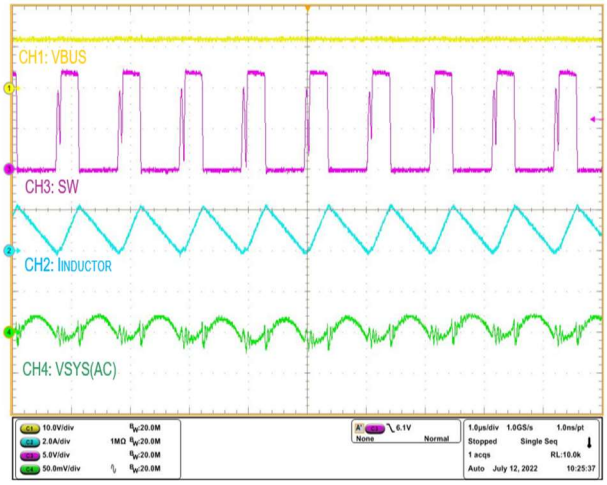


Fig10. Switching in Buck Mode
(Vbus=12V,Icharge=1A)

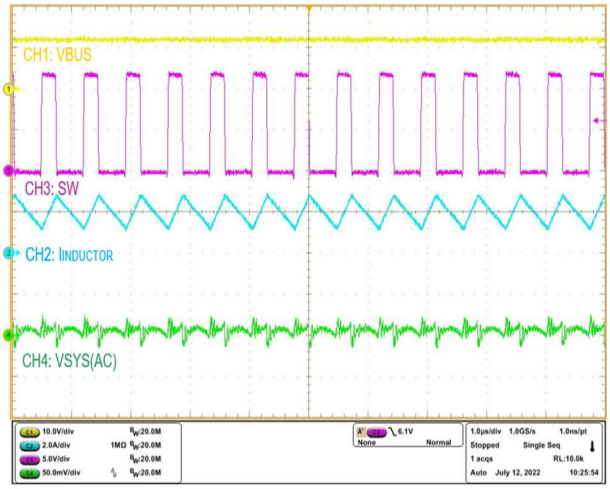


Fig11. Switching in Buck Mode
(Vbus=12V,Icharge=2A)

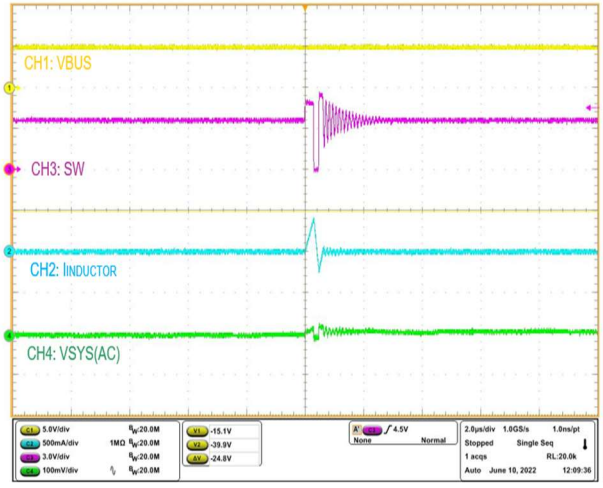


Fig12. VSYS Operation
(Vbus=5V,Vsys=3.6V,Isys=No Load)

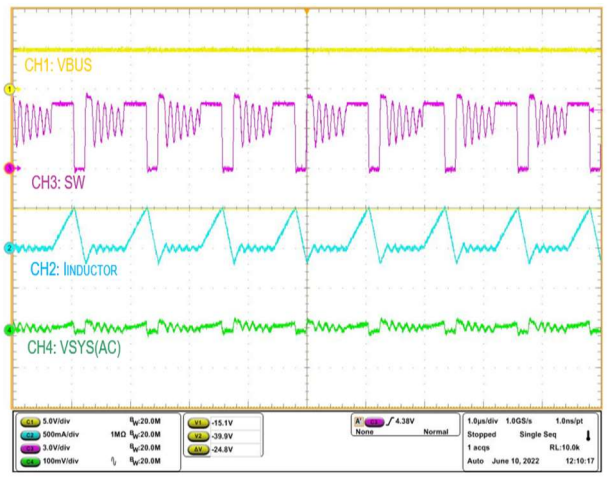


Fig13. VSYS Operation
(Vbus=5V,Vsys=3.6V,Isys=100mA)

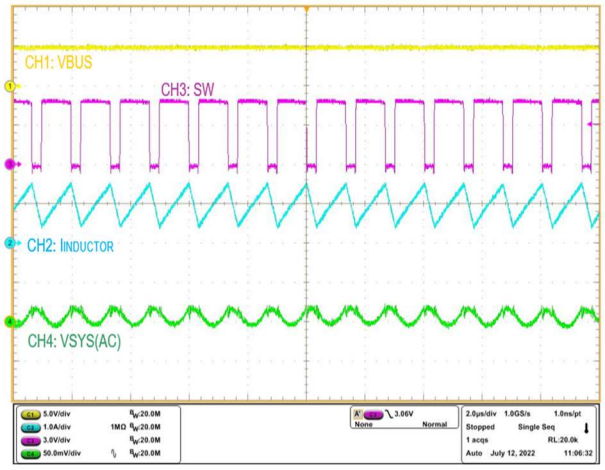


Fig14. VSYS Operation
(Vbus=5V,Vsys=3.6V,Isys=1A)

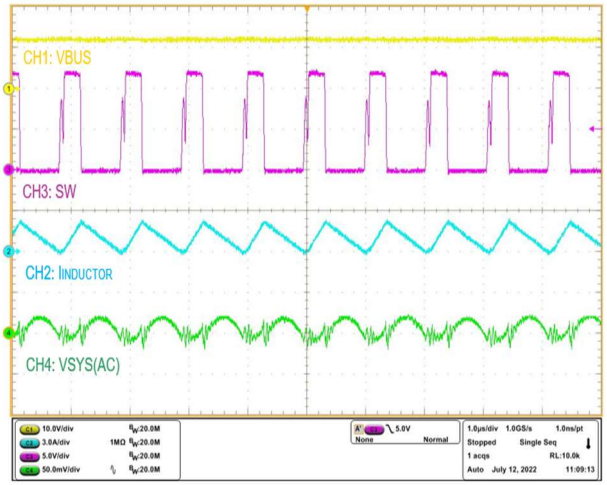


Fig15. VSYS Operation
(Vbus=12V,Vsys=3.6V,Isys=1A)

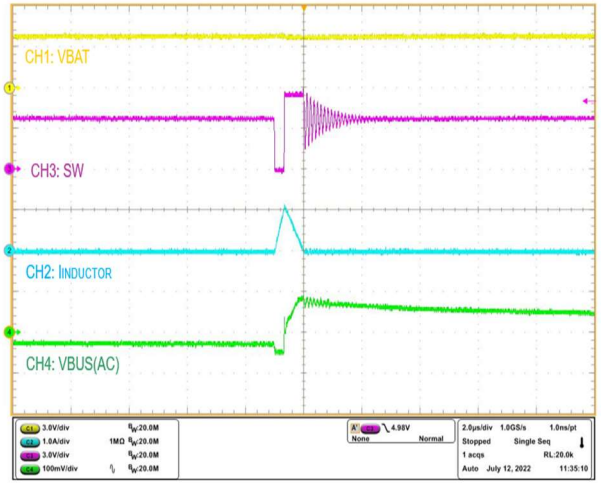


Fig16. OTG Switching
(Vbat=3.8V,Vbus=5.3V,No Load)

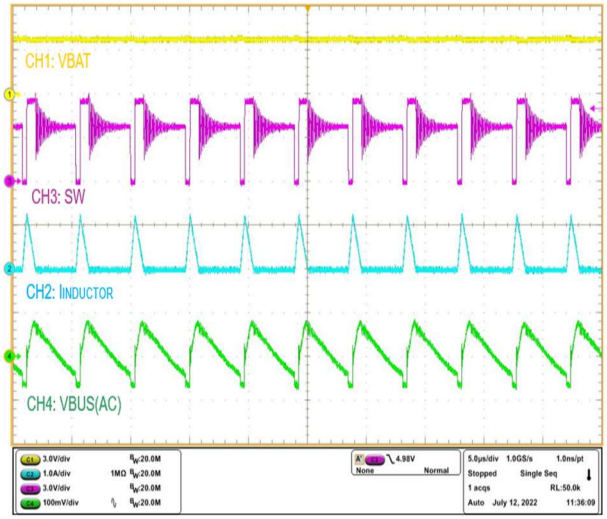


Fig17. OTG switching
(Vbat=3.8V,Vbus=5.3V,Iload=100mA)

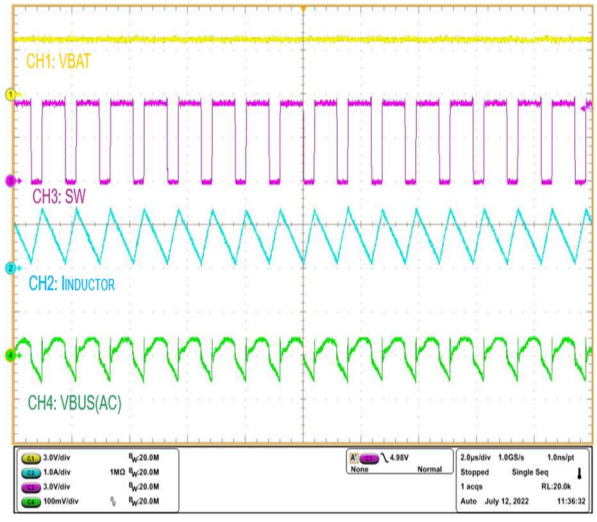


Fig18. OTG switching
(Vbat=3.8V,Vbus=5.3V,Iload=500mA)

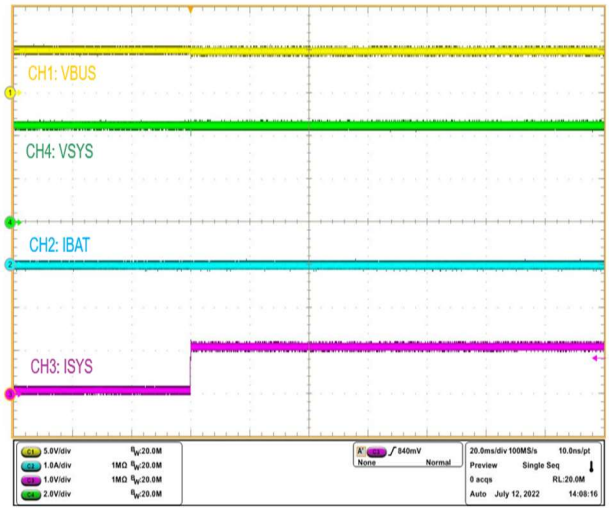


Fig19. System Load Transient
(Input is not over load, ISYS is only supported from BUS)

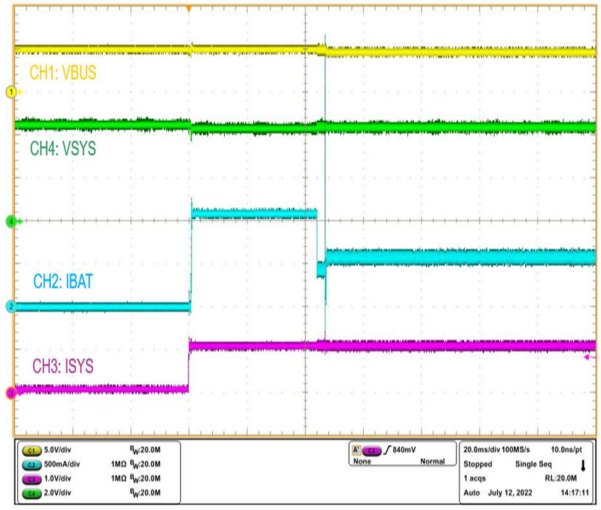


Fig20. System Load Transient
(Input is over load, ISYS is supported from both BUS and BAT)

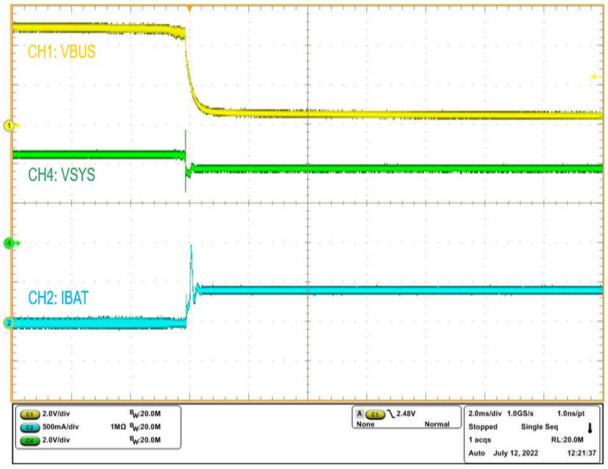


Fig21. System Load Transient
(Q4 turn on, ISYS supported from BAT after BUS input remove)

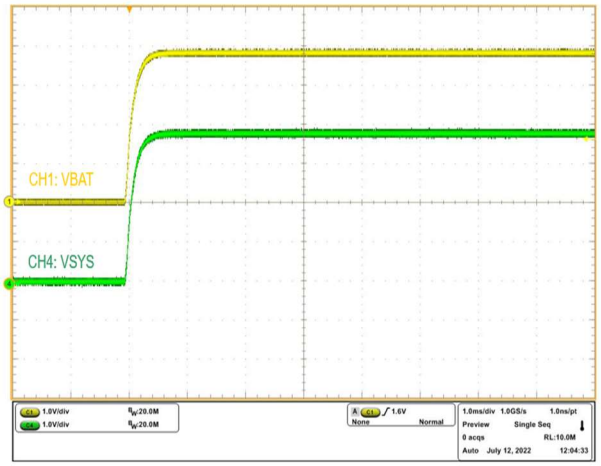


Fig22. System Start up from Battery
(No Load, VBUS Float)

6. Detailed Description

6.1 Circuit Overview

The PSC2965 is an I2C controlled power path management device and a single cell Li-Ion battery charger. It integrates the input reverse-blocking FET (RBFET, Q3), high-side switching FET (HSFET, Q1), low-side switching FET (LSFET, Q2), and battery FET (BATFET, Q4) between system and battery. The device also integrates the bootstrap diode for the high-side gate drive.

6.2 Function Block Diagram

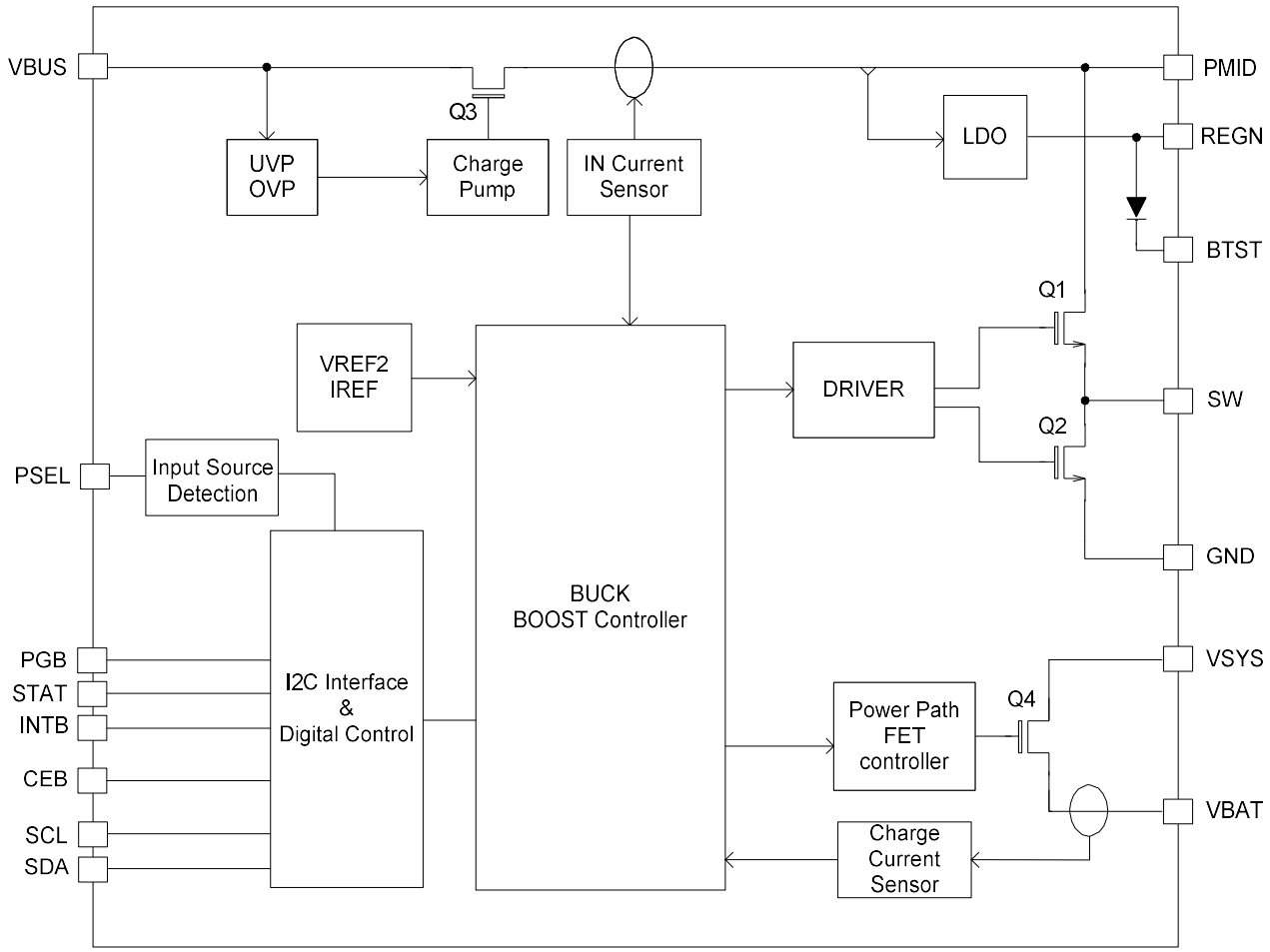


Figure 6.1 Block Diagram

6.3 Feature Description

6.3.1 Power Up from Battery without DC Source

When VBAT is powered up, the BATFET turns on and connects battery to system. The low RDSON in BATFET and the low quiescent current on BAT minimize the conduction loss and maximize the battery run time..

6.3.2 Interrupt to Host (INTB)

In some applications, the host does not always monitor the charger operation. The INT pulse notifies the systems on the device operation. The following events will generate 300us INT pulse.

- USB/adapter insertion and remove
- Charge complete
- NTC cold or hot detect
- 32s watchdog timer expire
- BAT temperature become abnormal or return to normal.

When a fault occurs, the charger device sends out INT and keeps the fault state in REG09 until all the faults are cleared. Before all the faults are cleared, the charger device would not send any INT upon new faults.

6.3.3 Shipping Mode

6.3.3.1 Enter Ship Mode

To extend battery life and minimize power when system is powered off during system idle, shipping, or storage, the device can turn off BATFET so that the system voltage is zero to minimize the leakage. The BATFET can be turned off by setting QOFF bit to “1”.

- Setting REG07[5](QOFF) to “1” allows the user to turn off the BATFET when the IC doesn’t work in charging mode and boost mode, but reset REG07[5] to “0” is invalid.
- In charging mode and boost mode, setting REG07[5] to “1” is invalid, but the BATFET can be turned off when VBAT is fully charged.

6.3.3.2 Exit Ship Mode

When the BATFET is disabled (in shipping mode) and indicated by setting QOFF, one of the following events can enable BATFET to restore system power:

1. Plug in adapter
2. Reset all by write “1” to REG0B[7];
3. A logic high to low transition on QONB pin with tSHIPMODE deglitch time to enable BATFET to exit shipping mode.

6.3.4 Power Path Management

6.3.4.1 Narrow VDC Architecture

The device deploys Narrow VDC architecture (NVDC) with BATFET separating system from battery. The minimum system voltage is set by REG01[3:1]. Even with a fully depleted battery, the system is regulated above the minimum system voltage (default 3.5 V).

When the battery is below minimum system voltage setting, the BATFET operates in linear mode (LDO mode), and the system is regulated at the minimum system voltage. As the battery voltage rises to Vsysmin-100mv, BATFET is fully turned on in switch mode.

When the battery is fully charged, the system is regulated at about VOREG+100mV.

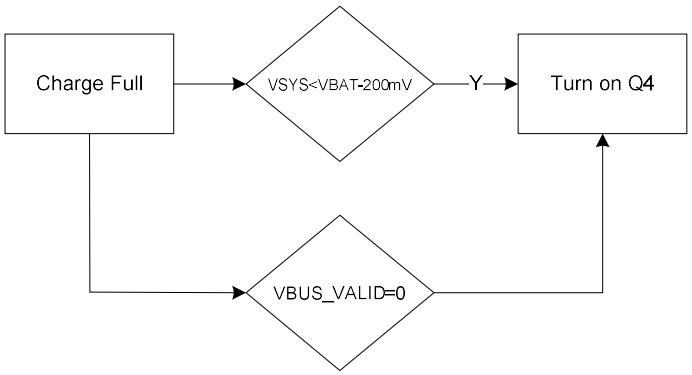
6.3.4.2 Dynamic Power Management

To meet maximum current limit in USB spec and avoid over loading the adapter, the device features Dynamic Power Management (DPM), which continuously monitors the input current and input voltage.

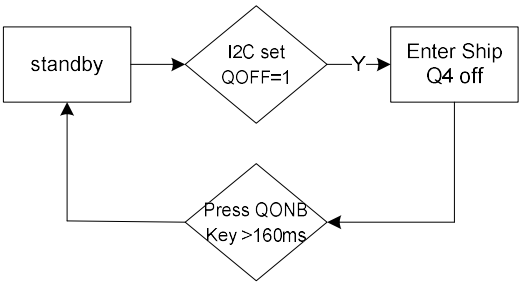
When input source is over-loaded, either the current exceeds the input current limit or the voltage falls below the input voltage limit. The device then reduces the charge current until the input current falls below the input current limit and the input voltage rises above the input voltage limit.

When the charge current is reduced to zero, but the input source is still overloaded, the device automatically enters the supplement mode. Battery starts discharging so that the system is supported from both the input source and battery.

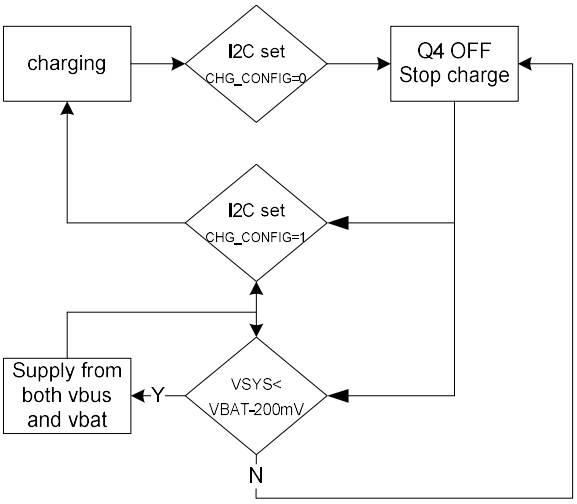
Charge done during system on



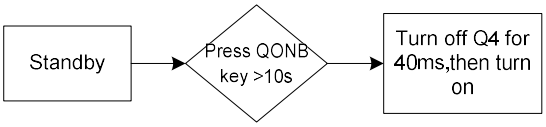
Ship mode



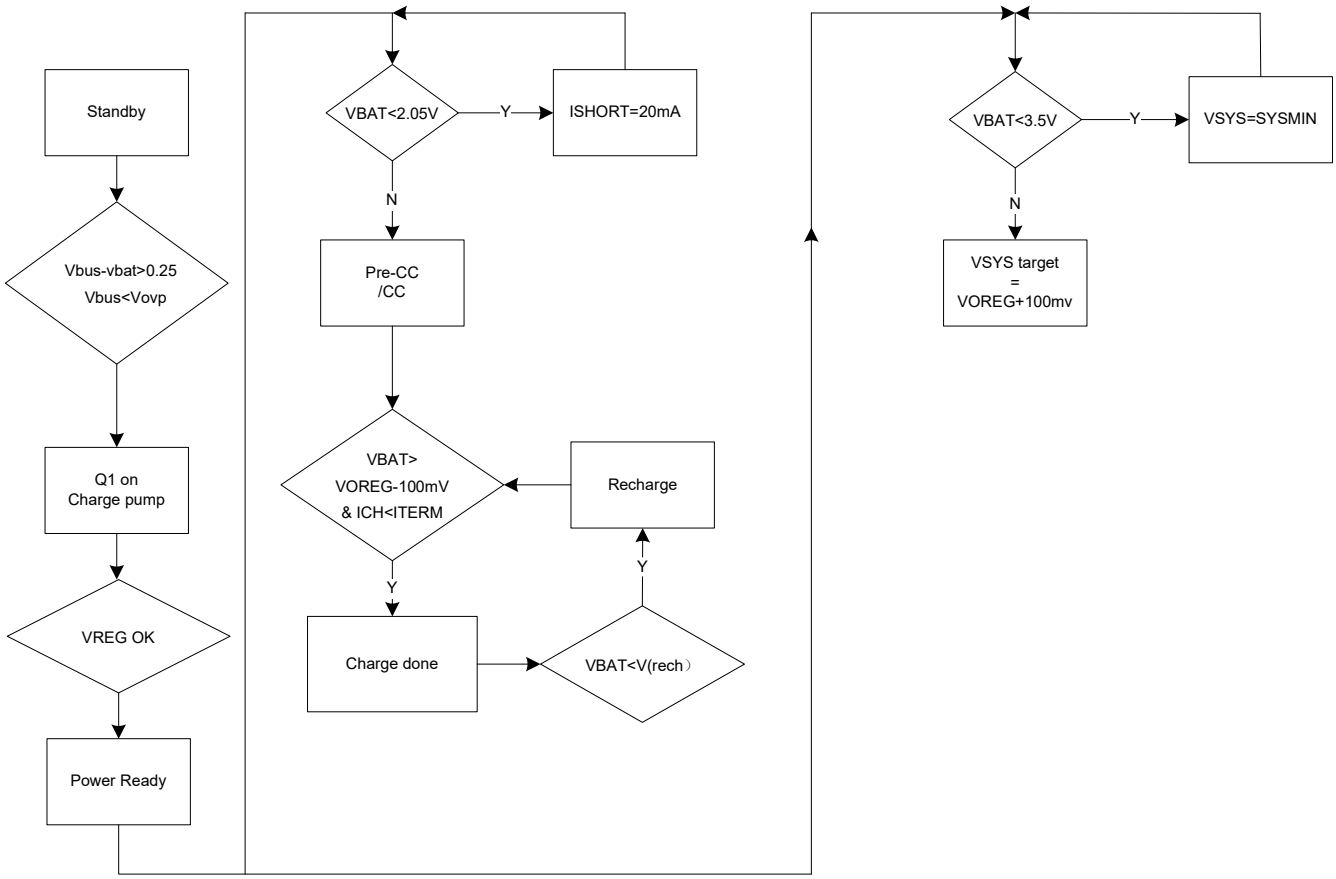
Turn off Q4 during charging



Force system reset



6.3.5 Charge Mode



6.3.5.1 Four Regulation Loops

1. Charging Current: Limits the maximum charging current. This current is sensed using internal BATFET.
2. Charge Voltage: The regulator is restricted from exceeding this voltage. As the internal battery voltage rises, the battery's internal impedance and BATFET work in conjunction with the charge voltage regulation to decrease the amount of current flowing to the battery. Battery charging is completed when the current thru BATFET drops below the I_{TERM} threshold.
3. Input Current: Limits the amount of current drawn from VBUS. This current is sensed internally and can be programmed through the I^2C interface.
4. Input Voltage: PSC2965 employ an additional loop to limit the amount of drop on VBUS to a programmable voltage (V_{SP}) to accommodate "special chargers" that limit current to a lower current than might be available from a "normal" USB wall charger.

6.3.5.2 Battery Charging Curve

The device charges the battery in four phases: activating, preconditioning, constant current, Fast-CC and constant voltage.

Charging Current Setting

VBAT	Charging Phase	Setting REG
$V_{BAT} < V_{SHORT}$ (Typical 2.05V)	ISHORT	-
$V_{SHORT} \le V_{BAT} < V_{WAKEUP}$ (Typical 2.05 V ≤ V_{BAT} < 3.1 V)	Pre-CC	REG03[7:4]
$V_{WAKEUP} \le V_{BAT}$ (Typical 3.1V ≤ V_{BAT} < Voreg)	CC	REG02[5:0]

Note: If the charger device is in DPM regulation during charging, the actual charging current will be less than the programmed value.

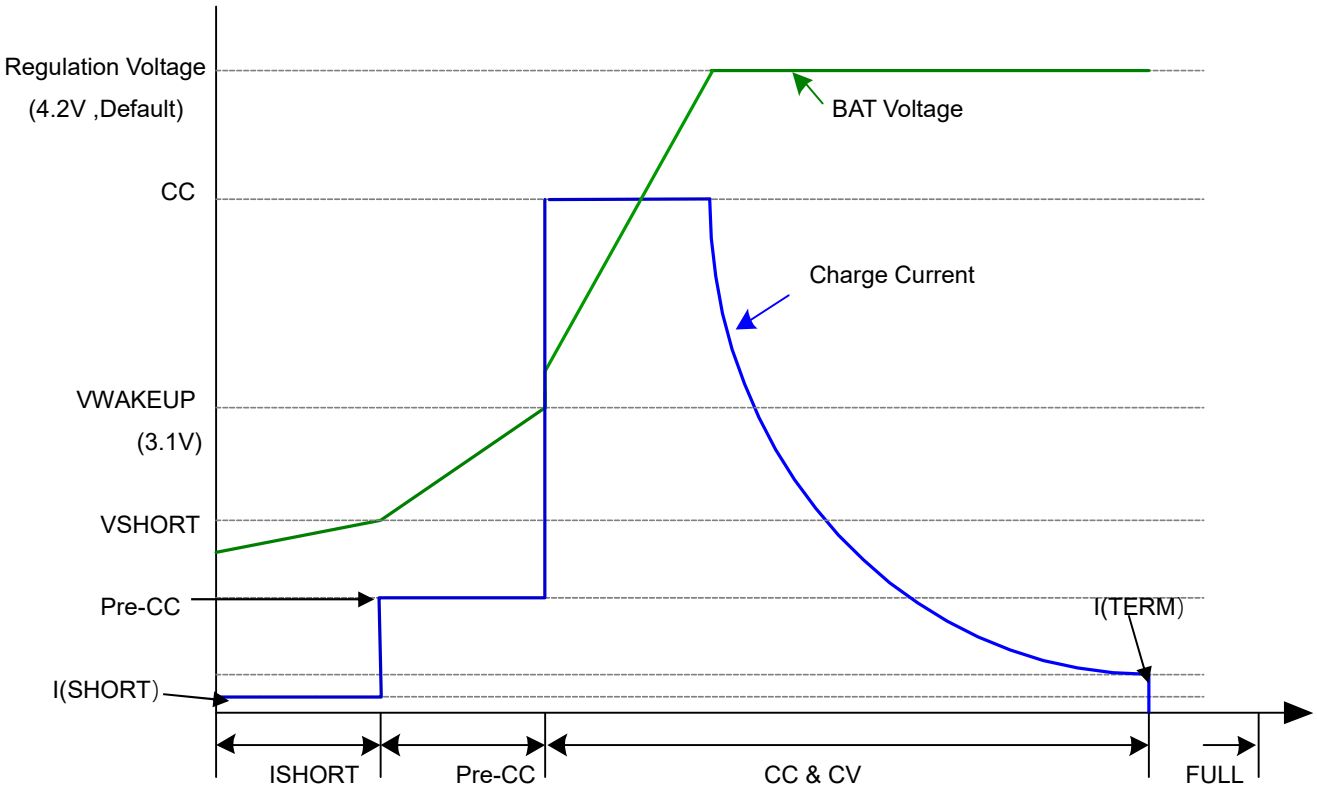


Figure 6.2 Charge Curve, I_{CHARGE} Not Limited by I_{INLIM}

6.3.5.3 Charge Termination

The device terminates a charge cycle when the battery voltage is above recharge threshold, and the current is below termination current. After the charging cycle is complete, the BATFET turns off. The converter keeps running to power the system, and BATFET can turn back on to engage supplement mode. When termination occurs, the status register REG08[4:3] is 11. Termination can be disabled by writing 0 to REG05[7].

The host can disable charging and VSYS power through CEB pin, or set REG01[4] to 0.Setting QOFF (REG07[5]) from 0 to 1 will cut VSYS from VBAT so as to disable charging, which won't impact VSYS supply.

6.3.5.4 Charger Safety Timer

The charger has a time out function for normal charge. For normal charging the timer is set to 12 hours. If the charger is still operating after typical 12 hours, BATFET will be turned OFF and will be turned on if the condition (VOREG-VBAT) >100mV is met, or plugging out the adapter.

The 12-hour timer can be reset by plugging out/in the adapter.

6.3.5.5 Charging Status Indicator (STAT)

The device indicates charging state on the open drain STAT pin. The STAT pin can drive LED as the application diagram shows.

--	STAT
VBUS is valid	LOW
NO valid VBUS	HIGH

6.3.5.6 Thermal Shutdown

During charge operation, the device monitors the internal junction temperature T_J to avoid overheat the chip and limits the IC surface temperature. When the internal junction temperature exceeds 140°C, the device is disabled, and is enabled if junction temperature lower than 120°C.

6.3.5.7 Input Over-Voltage Detection

When the VBUS exceeds $VBUS_{OVP}$, the IC suspends charging. When VBUS falls a hysteresis voltage below $VBUS_{OVP}$, the fault is cleared and charging resumes after VBUS is revalidated.

6.3.5.8 Battery Short Protection

If the battery voltage falls below V_{short} (2.4V typical), the device will turn off BATFET and keep 20mA linear charging current to VBAT.

6.3.5.9 JEITA

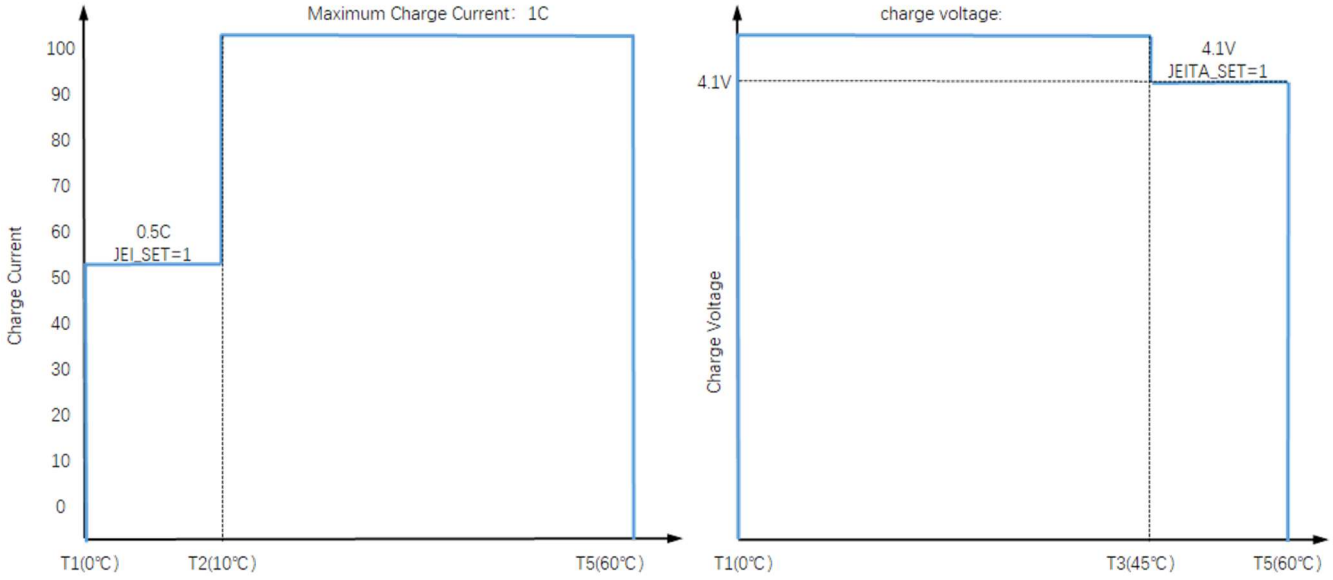
JEITA Guideline Compliance During Charging Mode

To improve the safety of charging Li-ion batteries, JEITA guideline was released on April 20, 2007. The guideline emphasized the importance of avoiding a high charge current and high charge voltage at certain low and high temperature ranges.

To initiate a charge cycle, the voltage on TS pin must be within the VT1 to VT5 thresholds. If TS voltage exceeds the T1-T5 range, the controller suspends charging and waits until the battery temperature is within the T1 to T5 range.

At cool temperature (T1-T2), JEITA recommends the charge current to be reduced to half of the charge current or lower. At warm temperature (T3-T5), JEITA recommends charge voltage less than 4.1 V.

The charger provides flexible voltage/current settings beyond the JEITA requirement. The voltage setting at warm temperature (T3-T5) can be VOREG or 4.1V (configured by JEITA_SET). The current setting at cool temperature (T1-T2) can be further reduced to 50% of fast charge current (JEITA_SET).

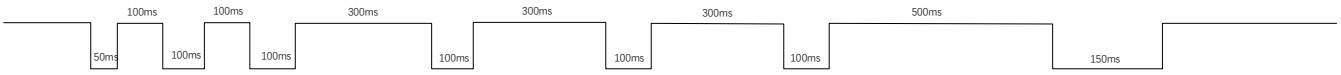


Note: 103AT as thermistor.

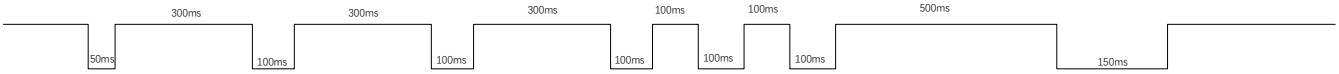
6.3.5.10 Current Pulse Modulation

The device includes interface to support adjustable high voltage adapter using input current pulse protocol.

Current pattern to request higher input voltage.



Current pattern to request lower input voltage;



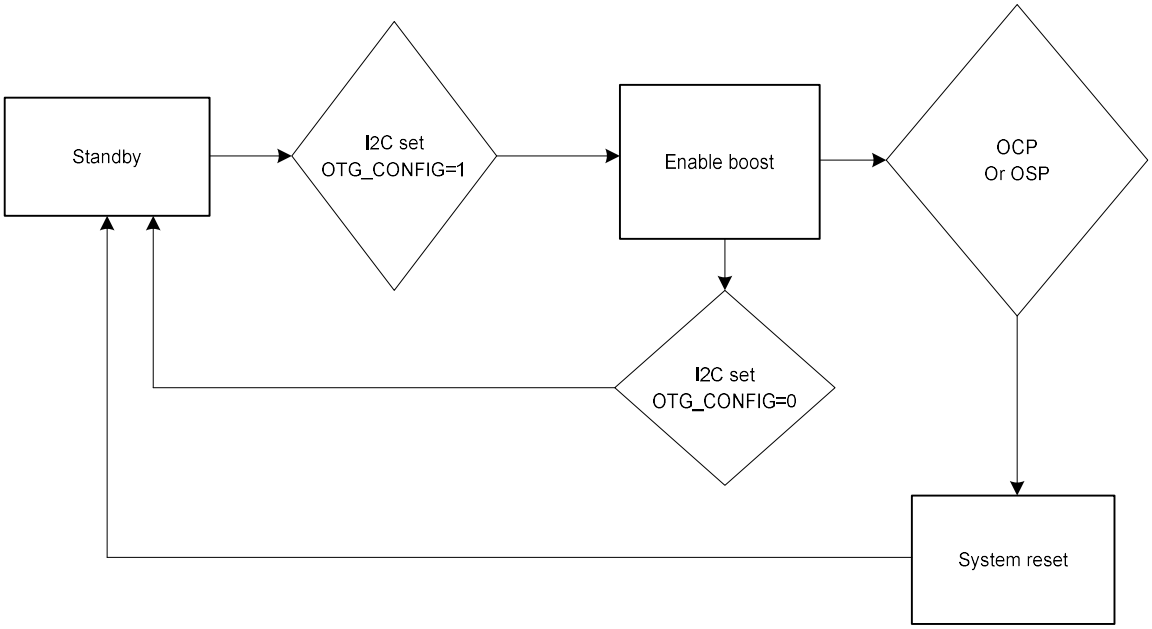
Current pulse can be programmed directly by control **DIS_PWM(REGA0[7])**.

6.3.6 Charger Parameters Description

Assuming that V_{OREG} is programmed to the cell's fully charged "float" voltage, the current that the battery accepts with the PWM regulator limiting its output (sensed at VBAT) to V_{OREG} declines, and the charger enters the voltage regulation phase of charging. When the current declines to the programmed I_{TERM} value, the charge cycle is complete. Charge current termination can be disabled by setting the TE bit (REG1[3]).
The charger output or "float" voltage can be programmed by the OREG bits from 3.6V to 4.45V as shown in REG02[6:4].

6.3.7 BOOST Mode

Boost Mode can be enabled by setting ENBOOST=1 through I2C. If there is valid VBUS, boost converter will be suspended.



6.3.7.1 Startup

When the boost regulator is shut down, current flow is prevented from V_{BAT} to V_{BUS}, as well as reverse flow from V_{BUS} to V_{BAT}.

6.3.7.2 Soft Start

This IC has built-in soft start function to prevent the IC being out of control. The reference voltage is slightly raised to the normal voltage within about 100us.

6.3.7.3 BST State

This is the normal operating mode of the regulator. The regulator uses a cot modulation scheme. The minimum t_{OFF} is proportional to $\frac{V_{IN}}{V_{OUT}}$ Which keeps the regulator's switching frequency reasonably constant in CCM.

To ensure the VBUS does not pump significantly above the regulation point, the boost switch remains off as long as FB > V_{REF}.

6.3.7.4 Over Current Protection

The device monitors the BATFET current to ensure safe boost mode operation. If over-current condition is detected, the device will lower the output voltage first. After about 400us, if it's still in over-current conditions, the device will reset and quit boost mode.

6.3.8 I2C Interface

The PSC2965's serial interface is compatible with Standard, Fast, Fast Plus, and High-Speed Mode I^2C-Bus® specifications. The PSC2965's SCL line is an input and its SDA line is a bi-directional open-drain output; it can only pull down the bus when active. The SDA line only pulls LOW during data reads and when signaling ACK. All data is shifted in MSB (bit 7) first.

Slave Address

The hex slave address for the PSC2965 is D6H.

Bus Timing

As shown in Figure 6.3, data is normally transferred when SCL is LOW. Data is clocked in on the rising edge of SCL. Typically, data transitions shortly at or after the falling edge of SCL to allow ample time for the data to set up before the next SCL rising edge.

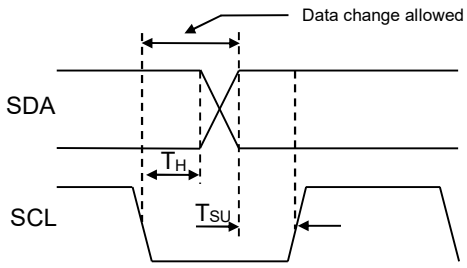


Figure 6.3 Data Transfer Timing

Each bus transaction begins and ends with SDA and SCL HIGH. A transaction begins with a START condition, which is defined as SDA transitioning from 1 to 0 with SCL HIGH, as shown in Figure 6.4.

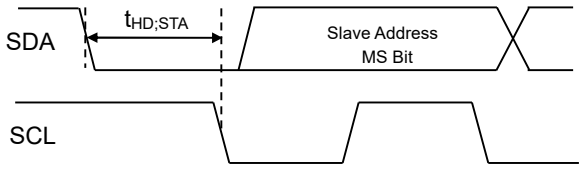


Figure 6.4 Start Bit

A transaction ends with a STOP condition, which is defined as SDA transitioning from 0 to 1 with SCL HIGH, as shown in Figure 6.5.

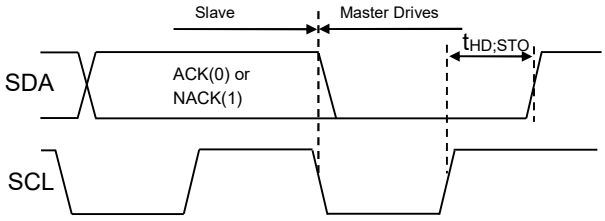


Figure 6.5 Stop Bit

During a read from the PSC2965, the master issues a Repeated Start after sending the register address and before resending the slave address. The Repeated Start is a 1-to-0 transition on SDA while SCL is HIGH, as shown in Figure 6.6.

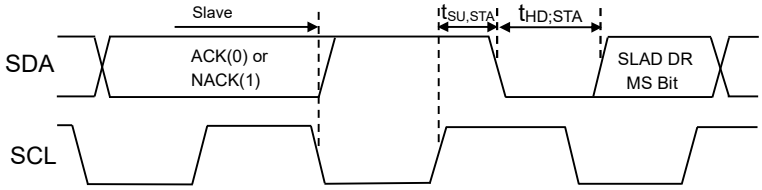


Figure 6.6 Repeated Start Timing

Read and Write Transactions

The figures below outline the sequences for data read and write. Bus control is signified by the shading of the packet, defined as Master Drives Bus and . Slave Drives Bus

All addresses and data are MSB first.

Bit Definitions for Figure 6.7, Figure 6.8

Symbol	Definition
S	START, see Figure 6.4
A	ACK. The slave drives SDA to 0 to acknowledge the preceding packet.
$\overline{A}$	NACK. The slave sends a 1 to NACK the preceding packet.
R	Repeated START, see Figure 6.6
P	STOP, see Figure 6.5

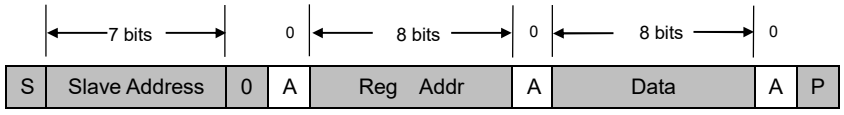


Figure 6.7 Write Transaction

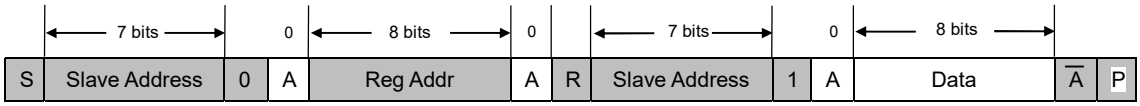


Figure 6.8 Read Transaction

Register Descriptions

Reg00

Bit	Field	POR	Type	Reset	Description	Comment
7	EN_HIZ	0	R/W	by REG_RST by Watchdog	0 – Disable, 1 – Enable	Enable HIZ Mode 0 – Disable (default) 1 – Enable
6	Reserved	0	R/W	by REG_RST by Watchdog	Reserved	Reserved
5	Reserved	0	R/W	by REG_RST by Watchdog	Reserved	Reserved
4	IINDPM[4]	1	R/W	by REG_RST	1600 mA	Current Limit Offset: 100 mA Range: 100 mA (000000) – 3.2 A (11111) Default: PSEL=Hi, 500mA (00100) PSEL=Lo,2400mA (10111), maximum input current limit, not typical. Host can't set current limit by writing IINDPM register bits when PSEL=H and PSEL_EN=1 (See description in Reg07[1]).
3	IINDPM[3]	0	R/W	by REG_RST	800 mA	
2	IINDPM[2]	1	R/W	by REG_RST	400 mA	
1	IINDPM[1]	1	R/W	by REG_RST	200 mA	
0	IINDPM[0]	1	R/W	by REG_RST	100 mA	

Reg01

Bit	Field	POR	Type	Reset	Description	Comment
7	Reserve	0	R/W	by REG_RST by Watchdog	Reserved	Reserved
6	WD_RST	0	R/W	by REG_RST by Watchdog	0 - Normal ; 1 - Reset	Default: Normal (0) Back to 0 after watchdog timer reset
5	OTG_CONFIG	0	R/W	by REG_RST by Watchdog	0 – OTG Disable 1 – OTG Enable	Default: OTG disable (0) Note: 1. OTG_CONFIG would over-ride Charge Enable Function in CHG_CONFIG
4	CHG_CONFIG	1	R/W	by REG_RST by Watchdog	0 - Charge Disable 1- Charge Enable	Default: Charge Battery (1) Note: 1. Charge is enabled when both CE pin is pulled low and CHG_CONFIG bit is 1.
3	SYS_Min[2]	1	R/W	by REG_RST	System Minimum Voltage	000-011: 3.2V 100: 3.4 V 101: 3.5 V 110: 3.6 V 111: 3.7 V Default: 3.5 V (101)
2	SYS_Min[1]	0	R/W	by REG_RST		
1	SYS_Min[0]	1	R/W	by REG_RST		
0	Reserved	0	R/W	by REG_RST by Watchdog	Reserved	Reserved

Reg02

Bit	Field	POR	Type	Reset	Description	Comment
7	BOOST_LIM	1	R/W	by REG_RST by Watchdog	0 = 0.8 A 1 = 1.5 A	Default: 1.5 A (1) Note: The current limit options listed are valley current limit specs.
6	Reserved	0	R/W	by REG_RST by Watchdog	Reserved	Reserved
5	ICHG[5]	1	R/W	by REG_RST by Watchdog	1920 mA	Fast Charge Current Default: 2040mA (100010) Range: 0 mA (0000000) – 3000 mA (110010) Note: I_{CHG} = 0 mA disables charge. I_{CHG} > 3000 mA (110010 clamped to register value 3000 mA (110010))
4	ICHG[4]	0	R/W	by REG_RST by Watchdog	960 mA	
3	ICHG[3]	0	R/W	by REG_RST by Watchdog	480 mA	
2	ICHG[2]	0	R/W	by REG_RST by Watchdog	240 mA	
1	ICHG[1]	1	R/W	by REG_RST by Watchdog	120 mA	
0	ICHG[0]	0	R/W	by REG_RST by Watchdog	60 mA	

Reg03

Bit	Field	POR	Type	Reset	Description	Comment
7	IPRECHG[3]	0	R/W	by REG_RST by Watchdog	480 mA	Precharge Current Default: 180 mA (0010) Offset: 60 mA Special Value: 1111: 0mA,disable precharge
6	IPRECHG[2]	0	R/W	by REG_RST by Watchdog	240 mA	
5	IPRECHG[1]	1	R/W	by REG_RST by Watchdog	120 mA	
4	IPRECHG[0]	0	R/W	by REG_RST by Watchdog	60 mA	
3	ITERM[3]	0	R/W	by REG_RST by Watchdog	800 mA	Termination Current Default: 300 mA (0010) Offset: 100 mA Maximum termination current : 800mA(1000)
2	ITERM[2]	0	R/W	by REG_RST by Watchdog	400 mA	
1	ITERM[1]	1	R/W	by REG_RST by Watchdog	200 mA	
0	ITERM[0]	0	R/W	by REG_RST by Watchdog	100 mA	

Reg04

Bit	Field	POR	Type	Reset	Description	Comment
7	VREG[4]	0	R/W	by REG_RST by Watchdog	512 mV	Charge Voltage Offset: 3.856V Special Value: 00000-00011: 3.984 V Range: 3.984V to 4.464 V (11000) Default: 4.208 V (01011) Special Value: 11000 -11111: 4.464V Clamped to register value 11000 (4.464 V)
6	VREG[3]	1	R/W	by REG_RST by Watchdog	256 mV	
5	VREG[2]	0	R/W	by REG_RST by Watchdog	128 mV	
4	VREG[1]	1	R/W	by REG_RST by Watchdog	64 mV	
3	VREG[0]	1	R/W	by REG_RST by Watchdog	32 mV	
2	TOPOFF_TIMER[1]	0	R/W	by REG_RST by Watchdog	00 – Disabled (Default) 01 – 150s 10 – 300s 11 – 450s	The extended time following the termination condition is met. When disabled, charge terminated when termination conditions are met
1	TOPOFF_TIMER[0]	0	R/W	by REG_RST by Watchdog		
0	VRECHG	0	R/W	by REG_RST by Watchdog	0 – 100 mV 1 – 200 mV	Recharge threshold Default: 100mV (0)

Reg05

Bit	Field	POR	Type	Reset	Description	Comment
7	EN_TERM	1	R/W	by REG_RST by Watchdog	0 – Disable 1 – Enable	Default: Enable termination (1)
6	Reserved	0	R/W	by REG_RST by Watchdog	Reserved	Reserved
5	Reserved	0	R/W	by REG_RST by Watchdog	Reserved	Reserved
4	Reserved	1	R/W	by REG_RST by Watchdog	Reserved	Reserved
3	WD_EN	1	R/W	by REG_RST by Watchdog	0 – Disable 1 – Enable watchdog timer	Default: Enable (1)
2	Reserved	1	R/W	by REG_RST by Watchdog	Reserved	Reserved
1	Reserved	1	R/W	by REG_RST by Watchdog	Reserved	Reserved
0	JEITA_ISET (0C-10C)	1	R/W	by REG_RST by Watchdog	0 – 50% of ICHG 1 – 20% of ICHG	Default: 20%

Reg06

Bit	Field	POR	Type	Reset	Description	Comment
7	OVP[1]	0	R/W	by REG_RST	Default: 6.8V (01)	VAC OVP threshold: 00 - 5.5 V 01 – 6.8 V (5-V input) 10 – 11 V (9-V input) 11 – 13.8 V (12-V input)
6	OVP[0]	1	R/W	by REG_RST		
5	BOOSTV[1]	1	R/W	by REG_RST		Boost Regulation Voltage: 00 - 4.85V 01 - 5.00V 10 - 5.15V 11 - 5.30V
4	BOOSTV[0]	0	R/W	by REG_RST		
3	VINDPM[3]	0	R/W	by REG_RST	800 mV	Absolute VINDPM Threshold Offset: 4.0 V Range: 4.0 V (0000) – 5.5 V (1111) Default: 4.6V (0110)
2	VINDPM[2]	1	R/W	by REG_RST	400 mV	
1	VINDPM[1]	1	R/W	by REG_RST	200 mV	
0	VINDPM[0]	0	R/W	by REG_RST	100 mV	

Reg07

Bit	Field	POR	Type	Reset	Description	Comment
7	PSEL_EN	0	R/W	by REG_RST by Watchdog	1 - Enable 0 - Disable	Default: Disable PSEL(0) PSEL_EN=1: IINLIM=500mA@PSEL = Hi; IINLIM is determined by the Reg 00[4:0]@ PSEL = Lo
6	Reserved	0	R/W	by REG_RST by Watchdog	Reserved	Reserved
5	BATFET_DIS	0	R/W	by REG_RST	0-Allow Q4 turn on, 1-Turn off Q4 with t_{BATFET_DLY} delay time (REG07[3])	Default: Allow Q4 turn on(0)
4	JEITA_VSET (45C-60C)	0	R/W	by REG_RST by Watchdog	0-Set Charge Voltage to 4.1V (max), 1-Set Charge Voltage to VREG	
3	BATFET_DLY	1	R/W	by REG_RST	0-Turn off BATFET immediately when BATFET_DIS bit is set 1-Turn off BATFET after t_{BATFET_DLY} (typ. 10 s) when BATFET_DIS bit is set	Default: 1 Turn off BATFET after t_{BATFET_DLY} (typ. 10 s) when BATFET_DIS bit is set
2	BATFET_RST_EN	1	R/W	by REG_RST by Watchdog	0-Disable BATFET reset function 1-Enable BATFET reset function	Default: 1 Enable BATFET reset function
1	VDPM_BAT_TRACK[1]	0	R/W	by REG_RST	00- Disable function (VINDPM set by register) 01- VBAT + 240mV 10- VBAT + 260mV 11- VBAT + 300mV	Sets VINDPM to track BAT voltage. Actual VINDPM is higher of register value and VBAT + VDPM_BAT_TRACK
0	VDPM_BAT_TRACK[0]	0	R/W	by REG_RST		

Reg08

Bit	Field	POR	Type	Reset	Description
7	VBUS_STAT[2]	x	R	NA	VBUS Status register 000: No input or in Boost mode 001: USB Host SDP (500 mA) 010: Adapter 2.4A Software current limit is reported in IINDPM register
6	VBUS_STAT[1]	x	R	NA	
5	VBUS_STAT[0]	x	R	NA	
4	CHRG_STAT[1]	x	R	NA	Charging status: By monitoring the voltage of battery 00 -Not Charging 01 - Pre-charge (< $V_{BATLOWV}$) 10 -Fast Charging 11 -Charge Termination
3	CHRG_STAT[0]	x	R	NA	
2	PG_STAT	x	R	NA	Power Good status: 0 – Power Not Good 1 – Power Good
1	THERM_STAT	x	R	NA	0 – Not in thermal regulation; 1 – in thermal regulation
0	VSYS_STAT	x	R	NA	0 – Not in VSYSMIN regulation (BAT > VSYSMIN) 1 – in VSYSMIN regulation (BAT < VSYSMIN)

Reg09

Bit	Field	POR	Type	Reset	Description
7	WATCHDOG_FAULT	x	R	NA	0 – Normal, 1- Watchdog timer expiration
6	BOOST_FAULT	x	R	NA	0 – Normal, 1 – VBUS overloaded in OTG, or battery is too low (any conditions that we cannot start boost function)
5	CHRG_FAULT[1]	x	R	NA	00 – Normal, 01 – input fault (OVP) or Thermal shutdown 11 – Charge Safety Timer Expiration
4	CHRG_FAULT[0]	x	R	NA	
3	Reserved	x	R	NA	
2	NTC_FAULT[2]	x	R	NA	JEITA 000 – Normal, 010 – Warm, 011 – Cool, 101 – Cold, 110 – Hot (Buck mode)
1	NTC_FAULT[1]	x	R	NA	
0	NTC_FAULT[0]	x	R	NA	

Reg0A

Bit	Field	POR	Type	Reset	Description
7	VBUS_GD	x	R	NA	0 – Not VBUS attached, 1 – VBUS Attached
6	VINDPM_STAT	x	R	NA	0 – Not in VINDPM, 1 – in VINDPM
5	IINDPM_STAT	x	R	NA	0 – Not in IINDPM, 1 – in IINDPM
4:0	Reserved	x	R	NA	

Reg0B

Bit	Field	POR	Type	Reset	Description
7	REG_RST	0	R/W	NA	Register reset 0 – Keep current register setting 1 – Reset to default register value and reset safety timer Note: Bit resets to 0 after register reset is completed
6	PN[3]	0	R	NA	
5	PN[2]	0	R	NA	
4	PN[1]	1	R	NA	
3	PN[0]	0	R	NA	
2	Reserved	0	R	NA	
1	DEV_REV[1]	0	R	NA	
0	DEV_REV[0]	0	R	NA	

Reg0C

Bit	Field	POR	Type	Reset	Description
4	NTC_DIS	0	R/W	by REG_RST by Watchdog	0:Enable NTC(default) 1:Disable NTC Note: The NTC_DIS must be set to 1 for high current(>2.0A) applications.

Reg0D

Bit	Field	POR	Type	Reset	Description
7:6	Charge Current Limit		R/W	by REG_RST by Watchdog	10： for Icharge<=2.0A 11： No charge current limit
0	Thermal_DIS	0	R/W	by REG_RST by Watchdog	0:Enable Thermal Regulation 1:Disable Thermal Regulation

7. PCB Layout Guidelines

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loop (see Figure 7.1) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Here is a PCB layout priority list for proper layout. Layout PCB according to this specific order is essential.

1. Place input capacitor as close as possible to PMID pin and GND pin connections and use shortest copper trace connection or GND plane.
2. Place inductor input pin to SW pin as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
3. Put output capacitor near to the inductor and the IC. Ground connections need to be tied to the IC ground with a short copper trace connection or GND plane.
4. Route analog ground separately from power ground. Connect analog ground and connect power ground separately. Connect analog ground and power ground together using thermal pad as the single ground connection point. Or using a 0Ω resistor to tie analog ground to power ground.
5. Use single ground connection to tie charger power ground to charger analog ground. Just beneath the IC. Use ground copper pour but avoid power pins to reduce inductive and capacitive noise coupling.
6. Decoupling capacitors should be placed next to the IC pins and make trace connection as short as possible.
7. It is critical that the exposed thermal pad on the backside of the IC package be soldered to the PCB ground.

Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers.

8. The via size and number should be enough for a given current path.

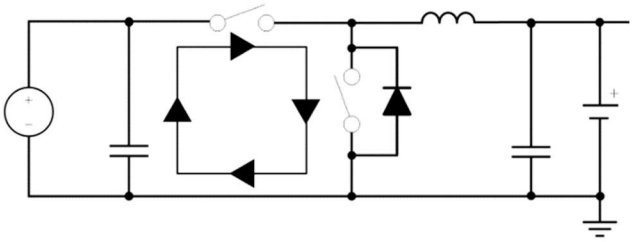
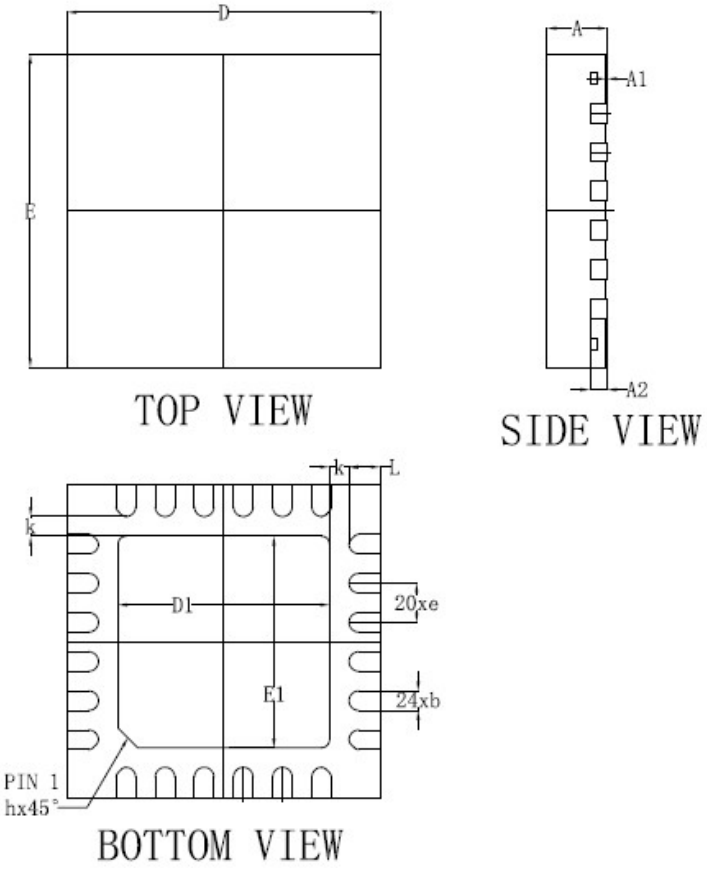


Figure 7.1 high frequency current path

8. Package Information



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.700	0.750	0.820
A1	0.000	/	0.050
A2	0.153	0.203	0.273
b	0.200	0.250	0.300
D	3.900	4.000	4.100
D1	2.600	2.700	2.800
E	3.900	4.000	4.100
E1	2.600	2.700	2.800
e	0.450	0.500	0.550
h	0.200	0.250	0.300
k	0.150	0.250	0.350
L	0.350	0.400	0.450

Ordering Information

Device	Package	Reel	Shipping
PSC2965	QFN4x4-24L (Pb-Free)	13"	5000 / Tape & Reel

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